

CLAIMS

What is claimed is:

1. A method for utilizing a signal delay model for
2 determining an interconnect delay at a node in an
3 interconnect having a plurality of nodes, said method
4 comprising:

5 determining an equivalent effective capacitance
6 value for a downstream load seen at said node; and

7 utilizing said equivalent effective capacitance
8 value to calculate said interconnect delay at said node.

1. The method as recited in Claim 1, further
2 comprising performing a bottom-up tree traversal to
3 compute the first three admittance moments for each of
4 said plurality of nodes in said interconnect.

1. The method as recited in Claim 1, wherein said
2 determining an equivalent effective capacitance value
3 includes determining interconnect delays for nodes in
4 said interconnect preceding said node.

1. The method as recited in Claim 1, wherein said
2 determining an equivalent effective capacitance includes
3 utilizing a pi-model to model said downstream load.

1. The method as recited in Claim 4, wherein said
2 determining an equivalent effective capacitance includes
3 determining an Elmore delay value for said node.

1. The method as recited in Claim 5, wherein said

2 equivalent effective capacitance (C_{eff}) is characterized
3 by:

4
$$C_{eff} = C_{fj} (1 - e^{-T/\tau_{dj}})$$

5 wherein C_{fj} is the far-end capacitance of said pi-model at
6 said node, T is the Elmore delay at said node and τ_{dj} is
7 the resistance of said pi-model (R_{dj}) multiplied by C_{fj} .

1 7. The method as recited in Claim 6, wherein said
2 utilizing said equivalent effective capacitance value
3 includes calculating said interconnect delay at said node
4 utilizing an effective capacitance metric (ECM) delay
5 model, wherein said ECM delay model is characterized by:

6
$$ECM_j = ECM_{p(j)} + R_j (C_j + C_{nj} + C_{fj} (1 - e^{-T/\tau_{dj}}))$$

7 wherein $ECM_{p(j)}$ is the computed ECM delay at the node
8 immediately preceding said node, R_j is the resistance
9 between said node and said preceding node, C_j is the
10 capacitance to ground at said node and C_{nj} is the near-end
11 capacitance of said pi-model at said node.

1 8. A data processing system, comprising:
2 a processor;
3 means for determining an equivalent effective
4 capacitance value for a downstream load seen at a node in
5 an interconnect having a plurality of nodes; and
6 means for utilizing said equivalent effective
7 capacitance value to calculate an interconnect delay at
8 said node.

1 9. The data processing system as recited in Claim
2 8, further comprising means for performing a bottom-up
3 tree traversal to compute the first three admittance
4 moments for each of said plurality of nodes in said
5 interconnect.

1 10. The data processing system as recited in Claim
2 8, wherein said means for determining an equivalent
3 effective capacitance value includes means for
4 determining interconnect delays for nodes in said
5 interconnect preceding said node.

1 11. The data processing system as recited in Claim
2 8, wherein said means for determining an equivalent
3 effective capacitance includes means for utilizing a pi-
4 model to model said downstream load.

1 12. The data processing system as recited in Claim
2 11, wherein said means for determining an equivalent
3 effective capacitance includes means for determining an
4 Elmore delay value for said node.

1 13. The data processing system as recited in Claim

2 12, wherein said equivalent effective capacitance (C_{eff})
3 is characterized by:

4
$$C_{eff} = C_{fj} (1 - e^{-T/\tau_{dj}})$$

5 wherein C_{fj} is the far-end capacitance of said pi-model at
6 said node, T is the Elmore delay at said node and τ_{dj} is
7 the resistance of said pi-model (R_{dj}) multiplied by C_{fi} .

1 14. The data processing system as recited in Claim
2 13, wherein said means for utilizing said equivalent
3 effective capacitance value includes means for
4 calculating said interconnect delay at said node
5 utilizing an effective capacitance metric (ECM) delay
6 model, wherein said ECM delay model is characterized by:

7
$$ECM_j = ECM_{p(j)} + R_j (C_j + C_{nj} + C_{fj} (1 - e^{-T/\tau_{dj}}))$$

8 wherein $ECM_{p(j)}$ is the computed ECM delay at the node
9 immediately preceding said node, R_j is the resistance
10 between said node and said preceding node, C_j is the
11 capacitance to ground at said node and C_{nj} is the near-end
12 capacitance of said pi-model at said node.

1 15. A computer program product, comprising:
2 a computer-readable medium having stored thereon
3 computer executable instructions for implementing a
4 method for determining an interconnect delay at a node in
5 an interconnect having a plurality of nodes, said
6 computer executable instructions when executed perform
7 the steps of:

8 determining an equivalent effective capacitance
9 value for a downstream load seen at said node; and
10 utilizing said equivalent effective capacitance
11 value to calculate said interconnect delay at said
120 node.

1 16. The computer program product as recited in
2 Claim 15, further comprising performing a bottom-up tree
3 traversal to compute the first three admittance moments
4 for each of said plurality of nodes in said interconnect.

1 17. The computer program product as recited in
2 Claim 15, wherein said determining an equivalent
3 effective capacitance value includes determining
4 interconnect delays for nodes in said interconnect
5 preceding said node.

1 18. The computer program product as recited in
2 Claim 15, wherein said determining an equivalent
3 effective capacitance includes utilizing a pi-model to
4 model said downstream load.

1 19. The computer program product as recited in
2 Claim 18, wherein said determining an equivalent
3 effective capacitance includes determining an Elmore

4 delay value for said node.

1 20. The computer program product as recited in
2 Claim 19, wherein said equivalent effective capacitance
3 (C_{eff}) is characterized by:

4
$$C_{eff} = C_{fj} (1 - e^{-T/\tau_{dj}})$$

5 wherein C_{fj} is the far-end capacitance of said pi-model at
6 said node, T is the Elmore delay at said node and τ_{dj} is
7 the resistance of said pi-model (R_{dj}) multiplied by C_{fi} .

1 21. The computer program product as recited in
2 Claim 20, wherein said utilizing said equivalent
3 effective capacitance value includes calculating said
4 interconnect delay at said node utilizing an effective
5 capacitance metric (ECM) delay model, wherein said ECM
6 delay model is characterized by:

$$ECM_j = ECM_{p(j)} + R_j (C_j + C_{nj} + C_{fj} (1 - e^{-T/\tau_{dj}}))$$

8 wherein $ECM_{p(j)}$ is the computed ECM delay at the node
9 immediately preceding said node, R_j is the resistance
10 between said node and said preceding node, C_j is the
11 capacitance to ground at said node and C_{nj} is the near-end
12 capacitance of said pi-model at said node.